PhD studentship (Full-time)

Institution	Xi'an Jiaotong-Liverpool University, China
School	School of CHIPS
Supervisors	Principal supervisor: Dr. Qifeng Lu (XJTLU) Co-supervisor: Prof. Wei Chen (XJTLU) Co-supervisor: Dr. Youbin Zheng (UoL)
Application Deadline	Open until the position is filled
Funding Availability	Funded PhD project (world-wide students)
Project Title	A study on the carrier transportation mechansim of self-alignment vertical structure flexible synpatic transistors for neuromorphic computing
Contact	Please email qifeng.lu@xjtlu.edu.cn with a subject line of the PhD project title. The principal supervisor's profile is linked here: https://scholar.xjtlu.edu.cn/en/persons/QifengLu

Requirements:

The candidate should have a first class or upper second class honours degree, or a master's degree (or equivalent qualification), in Microelectronics, Materials Science and related programme.

Evidence of good spoken and written English is essential. The candidate should have an IELTS score of 6.5 or above, if the first language is not English. This position is open to all qualified candidates irrespective of nationality.

Degree:

The student will be awarded a PhD degree from the University of Liverpool (UK) upon successful completion of the program.

Funding:

The PhD studentship is available for three years subject to satisfactory progress by the student. The award covers tuition fees for three years (currently equivalent to RMB 99,000 per annum). It also provides up to RMB 16,500 to allow participation at international conferences during the period of the award. The scholarship holder is expected to carry out the major part of his or her research at XJTLU in Suzhou, China. However, he or she is eligible for a research study visit to the University of Liverpool up to six months, if this is required by the project.

Project Description:

Vertical structure flexible synaptic transistors, capable of processing signals efficiently and insensitive to deformation, are of great significance to make a revolution in in-sensor computing and artificial intelligence. However, the existing vertical structure synaptic transistor based on two-dimensional (2D) material involves inter-layer transportation of carriers, which induces the uncontrollable channel current due to the random conduction path. Therefore, a self-alignment vertical structure synaptic transistor was proposed in this research. Benefited from the self-alignment design, the channel length can be controlled by the thickness of the insulator and the power consumption can be reduced by scaling the device. In addition, the carrier is confined in the same layer of the 2D material, which avoids the inter-layer transportation of the carriers, and the device stability can be enhanced. Therefore, the research outputs will build a foundation for neuromorphic sensory system.

For more information about doctoral scholarship and PhD programme at Xi'an Jiaotong-Liverpool University (XJTLU), please visit

https://www.xjtlu.edu.cn/en/admissions/global/entry-requirements/

https://www.xjtlu.edu.cn/en/admissions/global/fees-and-scholarship

How to Apply:

Interested applicants are advised to email qifeng.lu@xjtlu.edu.cn the following documents for initial review and assessment (please put the project title in the subject line).

- CV
- Two formal reference letters
- Personal statement outlining your interest in the position
- Certificates of English language qualifications (IELTS or equivalent)
- Full academic transcripts in both Chinese and English (for international students, only the English version is required)
- Verified certificates of education qualifications in both Chinese and English (for international students, only the English version is required)
- PDF copy of Master Degree dissertation (or an equivalent writing sample) and examiners reports available